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Title: LOW IMPEDANCE, HIGH-POWER SOCKET AND METHOD OF USING
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UNITED STATES PATENT APPLICATION

LOW IMPEDANCE, HIGH-POWER SOCKET AND METHOD OF USING

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Client Ref. No. P13264

LOW IMPEDANCE, HIGH-POWER SOCKET AND METHOD OF USING

FIELD OF THE INVENTION

The present invention relates to a microelectronic device power socket. More particularly, the present invention relates to a high-power socket for a microelectronic device such as a processor. In particular, the present invention relates to a low resistance path and optionally a low inductance path for power delivery through the socket.

BACKGROUND OF THE INVENTION

DESCRIPTION OF RELATED ART

Chip packaging requires high-power sockets for devices such as processors and application-specific integrated circuits (ASICs). A processor requires a high current to enable the multiple-gigahertz clock cycles that are being achieved and to enable the variety of logic and memory operations that are simultaneously being executed. High currents through sockets require low resistances in order to minimize power dissipation that is otherwise caused by resistance heating. Larger power dissipations in the socket result in higher socket temperatures, that in turn slow and ultimately defeat the device. Additionally a high inductance is often generated in the power socket. Overall, the impedance, the ratio of voltage to current also affects the performance of the microelectronic device. An unacceptably high impedance will degrade both the signal and increase the resistance heating. When such a heating problem occurs, processor speed is slowed, or worse, the device fails with the result of lost data and lost productivity.

One way to deal with the challenges created by high current draw is to use more input/output (I/O) pins for the current draw. This allows a larger cumulative cross-sectional area to carry the power current, but the result is added cost, and even more scarce I/O real estate on the footprint of the power socket. Further, where the number of pins added to the power dissipation load do not provide a significantly lowered resistance than the resistance of the pins in the more active regions of the processor, the effectiveness of the additional pins may not be sufficient to reduce the current flowing through a given region of the socket. Additionally, the added pins must provide an effective direct current (DC) shunt capability.

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which embodiments of the present invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention that are not necessarily drawn to scale and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is a top plan view of a high power socket according to an embodiment;

Figure 2A is a top plan view of a high power socket according to an embodiment;

Figure 2B is an elevational view of the socket depicted in Figure 2A;

Figure 2C is an elevational view of the socket depicted in Figure 2A;

Figure 3 is a perspective view of an inter-digital capacitor according to an embodiment;

Figure 4 is a perspective view of an inter-digital capacitor according to an embodiment;

Figure 5 is a top plan view of a high power socket according to an embodiment; and

Figure 6 is a method flow diagram according to an embodiment.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to a power socket for a microelectronic device such as a processor. In one embodiment, a low resistance and low inductance path is provided for power delivery through the power socket to the processor or microelectronic device that is being serviced by the power socket.

The following description includes terms, such as upper, lower, first, second, etc. that are used for descriptive purposes only and are not to be construed as limiting. The embodiments of a device or article of the present invention described herein can be manufactured, used, or shipped in a number of positions and orientations. The terms "die" and "processor" generally refer to the physical object that is the basic workpiece that is transformed by various process operations into the desired integrated circuit. A die is typically made of semiconductive material that has been singulated from a wafer after integrated processing. Wafers may be made of semiconducting, non-semiconducting, or combinations of semiconducting and non-semiconducting materials.

Reference will now be made to the drawings wherein like structures will be provided with like reference designations. In order to show the structures of the present invention most clearly, the drawings included herein are diagrammatic representations of inventive articles. Thus, the actual appearance of the fabricated structures, for example in a photomicrograph, may appear different while still incorporating the essential structures of the present invention.

Moreover, the drawings show only the structures necessary to understand the present invention. Additional structures known in the art have not been included to maintain the clarity of the drawings.

Figure 1 illustrates a high-current power socket 10. The power socket 10 includes a socket platform 12 including a major planar surface that is depicted in the X-Y plane. A first power terminal 14 is disposed on the socket platform 12 and is spaced apart from a first ground terminal 16 along an upper edge 18. The first power terminal 14 includes a first cross-sectional area that is defined by a power terminal height 20 and a power terminal width 22. The power socket 10 also includes an input/output (I/O) pin socket 24 that includes a second cross-sectional area defined by an I/O pin socket height 26 and an I/O pin socket width 28. It is noted that the first cross-sectional area is larger than the second cross-sectional area. In one embodiment the ratio of the first cross-sectional area to the second cross-sectional area is from about 4:1 to about 50:1. In another embodiment, the ratio is from about 8:1 to about 40:1. In another embodiment, it is from about 16:1 to about 30:1. This cross-sectional area comparison may be a comparison of height 20 multiplied by the width 22, compared to the cross-sectional area of a pin (not pictured) that inserts into I/O pin socket 24 from a device such as an interposer (not pictured). The cross-sectional area may also be the surface area of contact within the locking mechanism (not pictured) within the I/O pin socket 24 as is known in the art.

In one embodiment, besides the first power terminal 14 and the first ground terminal 16, the power socket 10 includes a second power terminal 30 and a second ground terminal 32. Additionally in this embodiment as can be seen, a plurality of I/O pin sockets are provided that are substantially similar to the I/O pin socket 24. In addition to the structure of power socket 10, a center space 34 is provided in one embodiment for a power capacitor for delivering short-range

power to the electronic device. In this embodiment, center space 34 is provided for a land-side capacitor (LSC).

Figure 2 illustrates another embodiment of a power socket 110. In some applications, a lower inductance is desired during power delivery to an electronic device such as a general processor or an ASIC. The power socket 110 includes structures that are similar to the power socket 10 depicted in Figure 1. A first power terminal 14 is disposed on a socket platform 112 and is spaced apart from a first ground terminal 16 along an upper edge 118. Additionally, a first plurality of I/O pin sockets 24 is provided.

Where the bulk of the power current supplied to the electronic device passes first through the power terminals 14 and 30, and passes to ground through the ground terminals 16 and 32, significant inductance may result for some applications. According to this embodiment, current is also allowed to pass through a capacitor structure as illustrated generically by item 136. The capacitor structure 136 is oriented such that its capacitative surfaces (*e.g.* capacitor plates) are arranged orthogonal to the X-Y plane. In other words, the capacitor plates are vertically oriented to the major planar surface. In one embodiment, the capacitor structure 136 includes an inter-digital capacitor (illustrated in various embodiments in Figures 3 and 4). The inter-digital capacitor includes capacitor plates that are vertically (orthogonally) oriented to the major planar surface that is defined by the X-Y plane. Optionally and additionally, a second capacitor 138 that may be an inter-digital capacitor is disposed between second power terminal 30 and second ground terminal 32 at a lower edge 140 of power socket 110.

Figure 2B is an elevational view of power socket 110, taken along the line 2B -- 2B from Figure 2A. Power socket 110 in this view includes a major planar upper surface 142 and a major planar lower surface 144. Figure 2B illustrates that both power 30 and ground 32 terminals

extend below major planar lower surface 144, as well as second capacitor 138. The degree to which the power and ground terminals as well as the capacitor(s) extend below major planar lower surface 144 is often determined by a specific application of the embodiment.

Figure 2C is an elevational view of power socket 110, taken along the line 2C -- 2C from Figure 2A. Power socket 110 in this view includes the major planar upper surface 142 and the major planar lower surface 144. Figure 2C illustrates that both ground terminals 32 and 16 as they extend below major planar lower surface 144. Figure 2C also illustrates a second plurality of electrical bumps 150 disposed at the major planar lower surface 144. In one embodiment, the bumps 150 are mounted on a bond pad 152. In one embodiment, the bond pad 152 is set flush (not pictured) with the major planar lower surface 144. In one embodiment, the second plurality of electrical bumps 150 is equal to the first plurality of I/O pin sockets 24, depicted in Figure 2A.

Figure 3 is a perspective view of an inventive inter-digital capacitor IDC 310 that is used in an embodiment of the invention. In this embodiment, a first capacitor plate 312 is assigned a power plate designation. First power capacitor plate 312 is connected to a first power connector 314, and a second power connector 316 at the top side thereof, and electrical connection is made by a first power tab 318 and a second power tab 320. At the bottom side thereof, first power capacitor plate 312 is connected to a third power connector 322, and a fourth power connector 324 at the bottom side thereof, and electrical connection is made by a third power tab 326 and a fourth power tab 328. By this configuration, first power tab 318 is most closely connected from the top to the bottom of IDC 310, diagonally across first power capacitor plate 312 to fourth power tab 328. This diagonal proximity may be referred to as a first polarity type.

A second capacitor plate 330 is assigned a ground plate designation. Second ground capacitor plate 330 is connected to a first ground connector 332, a second ground connector 334

at the top side thereof, and electrical connection is made by a first ground tab 336 and a second ground tab 338. At the bottom side thereof, second ground capacitor plate 330 is connected to a third ground connector 340, and a fourth ground connector 342 at the bottom side thereof, and electrical connection is made by a third ground tab 344 and a fourth ground tab 346. Accordingly the inventive IDC includes a series of alternating power and ground connectors on the top side and on the bottom side. The power and ground connectors are configured to make a connection with other structures such as an interposer on one side and a board on the other side.

It is noted that a plurality of alternating power and ground plates are depicted. According to an embodiment, the number of power and ground plates is in a range from about 4 to about 10,000 or more, depending upon the thickness of the plates and the totality of space in the X-dimension. In one embodiment, the number of power and ground plates is in a range from about 100 to about 2,000. In one embodiment, the number of power and ground plates is in a range from about 400 to about 800. In one embodiment, spacing between a given power capacitor plate and a given ground capacitor plate is in a range from about 0.1 mil to about 0.5 mils. In another embodiment, the spacing is about 0.3 mils.

A dielectric material (not pictured) is placed between first power capacitor plate 312 and second ground capacitor plate 330. In one embodiment, the dielectric material is silica. In one embodiment, the dielectric material is a low-K (meaning having a dielectric constant lower than that of silica) such as SiLK® made by Dow Chemical of Midland, Michigan, or FLARE® made by AlliedSignal Inc. of Morristown, NJ.

Figure 4 is a perspective view of another IDC 410 according to an embodiment. In this embodiment, a first capacitor plate 412 is assigned a power plate designation. First power capacitor plate 412 is connected to a first power connector 414, and a second power connector

416 at the top side thereof, and electrical connection is made by a first power tab 418 and a second power tab 420. At the bottom side thereof, first power capacitor plate 412 is connected to a third power connector 422, and a fourth power connector 424 at the bottom side thereof, and electrical connection is made by a third power tab 426 and a fourth power tab 428. By this configuration, first power tab 418 is most closely connected from the top to the bottom of IDC 410, substantially vertically across first power capacitor plate 412 to fourth power tab 428. This substantially vertical proximity may be referred to as a second polarity type.

A second capacitor plate 430 is assigned a ground plate designation. Second ground capacitor plate 430 is connected to a first ground connector 432, a second ground connector 434 at the top side thereof, and electrical connection is made by a first ground tab 436 and a second ground tab 438. At the bottom side thereof, second ground capacitor plate 430 is connected to a third ground connector 440, and a fourth ground connector 442 at the bottom side thereof, and electrical connection is made by a third ground tab 444 and a fourth ground tab 446.

It is noted that a plurality of alternating power and ground plates are depicted. According to an embodiment, the number of power and ground plates is in a range from about 2 to about 10,000 or more, depending upon the thickness of the plates and the totality of space in the X-dimension. Other ground and power capacitor plate number ranges are set forth herein. In one embodiment, spacing between a given power capacitor plate and a given ground capacitor plate is in a range from about 0.1 mil to about 0.5 mils. In another embodiment, the spacing is about 0.3 mils.

As set forth herein, a dielectric material (not pictured) is placed between first power capacitor plate 412 and second ground capacitor plate 430.

Figure 5 depicts another embodiment in which the arrangement of power and ground terminals is rotated in relation to the vertical capacitors. A power socket 510 includes a first power terminal 514 embedded in a socket platform 512 and is spaced apart from a second power terminal 530 along an upper edge 518. Additionally, a first plurality of I/O sockets 524 is provided. The major planar surface of power socket 510 is depicted in the X-Y plane. A first ground terminal 516 and a second ground terminal 532 are spaced apart along a lower edge 540. In addition to the structure of power socket 510, a center space 534 is provided in one embodiment for a power capacitor for delivering short-range power to the electronic device. In this embodiment, center space 534 is provided for an LSC.

By this embodiment, current is also allowed to pass through a capacitor structure as illustrated generically by item 536. The capacitor structure 536 is disposed between the first power terminal 514 and the second power terminal 530. The capacitor structure 536 is oriented such that its capacitative surfaces (*e.g.* capacitor plates) are arranged orthogonal to the X-Y plane. In other words, the capacitor plates are vertically oriented to the major planar surface. In one embodiment, the capacitor structure 536 includes an inter-digital capacitor (illustrated in various embodiments in Figures 3 and 4). The inter-digital capacitor includes capacitor plates that are vertically (orthogonally) oriented to the major planar surface that is defined by the X-Y plane. Optionally and additionally, a second inter-digital capacitor 538 is disposed between the first ground terminal 516 and the second ground terminal 532 at the lower edge 540 of power socket 110. It is noted in Figure 5 that the IDCs 310 or 410 may be used as an embodiment in the location of capacitors 536 and 538.

By recitation of these embodiments, it should be noted that the placement of both the power and ground terminals as well as the capacitor with vertically oriented capacitor plates,

may be substantially anywhere on the socket platform 512 as well as for the embodiment of the socket platform 12 (Figure 1, for terminals only) and platform 112 (Figure 2A). However, where the I/O pin sockets 524 may be optimally located directly below the processor or other microelectronic device, the location of the power and ground terminals as well as the capacitor, in one embodiment, is along the periphery of the socket platform 512.

According to a method embodiment, a method of operating a device is depicted in **Figure 6**. The method commences by passing 610 a current through a power socket. The current may include an alternating first current and a direct second current. The alternating first current passes 620 in a first direction through a first capacitor plate that is configured in a plane collinear with the first direction. The direct second current passes 630 in the first direction through a power terminal. At certain frequencies, the alternating first current discharges 640 into a second capacitor plate and conducts in a second direction that is substantially opposite to the first direction. For example, the frequency is in a range from about 1 GHz to about 10 GHz. As set forth herein, the second capacitor plate is spaced apart and immediately adjacent the first capacitor plate. Because of the proximity of the first and second capacitor plates and the vertical loop inductance, surrounded by the plurality of power and ground plates, results in an inductance in a range below about 0.1 pico Henry/square. In another embodiment, the inductance is from about 0.01 pico Henry/square to about 0.06 pico Henry/square. In another embodiment, the inductance is about 0.03 pico Henry/square. Further operations in the method include the direct second current passing to ground 650 through a ground terminal in the second direction. One advantage of this embodiment is that the overall impedance is reduced by the concerted presence of the power and ground terminal(s) and the vertically oriented capacitor(s).

The following is a method example. Reference may be made to the structure depicted in Figures 2A - 2C. A DC current in the range from about 30 Ampere to about 200 Ampere passes through power terminals 14 and 30. An AC current in the range from about 10 milli Ampere to about 10 Ampere passes through the vertical capacitors 136 and 138 at a frequency of in a range from about 100 MHz to about 20 GHz. Total inductance in power socket 110 is in a range from about 0.1 picoHenry to about 10 picoHenry. Total resistance is in a range from about 2 milli Ohms to about 8 milli Ohms.

It will be readily understood to those skilled in the art that various other changes in the details, material, and arrangements of the parts and method stages which have been described and illustrated in order to explain the nature of this invention may be made without departing from the principles and scope of the invention as expressed in the subjoined claims.

CLAIMS

What is claimed is.

1. A power socket comprising:

a socket platform including a major planar surface; and on the socket platform:

a power terminal spaced apart from a ground terminal, wherein the power terminal includes a first cross-sectional area; and

an input/output (I/O) pin socket, wherein the I/O pin socket includes a second cross-sectional area that is smaller than the first cross-sectional area.

2. The power socket according to claim 1, on the socket platform further including:

a capacitor that has capacitor plates vertically oriented to the major planar surface.

3. The power socket according to claim 1, on the socket platform further including:

an inter-digital capacitor that has capacitor plates vertically oriented to the major planar surface.

4. The power socket according to claim 1, wherein the socket platform includes a first edge and a second edge, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, and wherein the two ground terminals are symmetrically disposed along the second edge.

5. The power socket according to claim 1, wherein the socket platform includes a first edge and a second edge, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, wherein the two ground terminals are symmetrically disposed along the second edge; and

a capacitor that is vertically oriented to the major planar surface and that is disposed between one of the power terminals and one of the ground terminals.

6. The power socket according to claim 1, wherein the socket platform includes a first edge and a second edge, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, wherein the two ground terminals are symmetrically disposed along the second edge; and

a capacitor that is vertically oriented to the major planar surface and that is disposed either between the two power terminals or the two ground terminals.

7. The power socket according to claim 1, further:

wherein the socket platform includes a first edge and a second edge;

wherein the power terminal includes a first power terminal and a second power terminal;

wherein the ground terminal includes a first ground terminal and a second ground terminal;

wherein the capacitor includes a first capacitor and a second capacitor;

wherein the first and second power terminals are symmetrically disposed along the first edge;

wherein the first and second ground terminals are symmetrically disposed along the second edge;

wherein the first and second capacitors are vertically oriented to the major planar surface;

wherein the first capacitor is disposed between the first power terminal and the first ground terminal; and

wherein the second capacitor is disposed between the second power terminal and the second ground terminal.

8. The power socket according to claim 1, further:

wherein the socket platform includes a first edge and a second edge;

wherein the power terminal includes a first power terminal and a second power terminal;

wherein the ground terminal includes a first ground terminal and a second ground terminal;

wherein the capacitor includes a first capacitor and a second capacitor;

wherein the first and second power terminals are symmetrically disposed along the first edge;

wherein the first and second ground terminals are symmetrically disposed along the second edge;

wherein the first and second capacitors are vertically oriented to the major planar surface;

wherein the first capacitor is disposed between the first power terminal and the second power terminal; and

wherein the second capacitor is disposed between and the first ground terminal and the second ground terminal.

9. The power socket according to claim 1, wherein the I/O pin socket is part of a plurality of pin sockets.

10. The power socket according to claim 1, wherein the capacitor includes an inter-digital capacitor of a first polarity type.

11. The power socket according to claim 1, wherein the capacitor includes an inter-digital capacitor of a second polarity type.

12. A power socket comprising:

a major planar upper surface and a major planar lower surface;

a power terminal spaced apart from a ground terminal, wherein the power terminal includes a first cross-sectional area;

a first plurality of input/output (I/O) pin sockets disposed at the major planar upper surface, wherein I/O pin socket of the plurality of I/O pin sockets includes a second cross-sectional area that is smaller than the first cross-sectional area;

a capacitor that has capacitor plates vertically oriented to the major planar surface; and

a second plurality of electrical bumps disposed at the major planar lower surface.

13. The power socket according to claim 12, wherein the second plurality of electrical bumps equals the first plurality of I/O pin sockets.

14. The power socket according to claim 12, wherein the capacitor includes an inter-digital capacitor.

15. The power socket according to claim 12, wherein the socket platform includes a first edge and a second edge, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, and wherein the two ground terminals are symmetrically disposed along the second edge.

16. The power socket according to claim 12, wherein the socket platform includes a first edge and a second edge, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, wherein the two ground terminals are symmetrically disposed along the second edge; and

wherein the capacitor includes a first and a second inter-digital capacitor that are vertically oriented to the major planar surface, and wherein the first inter-digital capacitor is disposed between one of the power terminals and one of the ground terminals.

17. A power socket comprising:

a plurality of input/output (I/O) pin sockets embedded in a socket platform, wherein the socket platform includes a major planar surface;

a power terminal embedded in the socket platform;

a ground terminal embedded in the socket platform; and

a capacitor embedded in the socket platform, wherein the capacitor includes a power plate and a ground plate, and wherein the power plate and the ground plate are configured orthogonal to the major planar surface.

18. The power socket according to claim 17, wherein the capacitor includes an inter-digital configuration.

19. The power socket according to claim 17, wherein the capacitor includes an inter-digital configuration including a plurality of power and ground plates, and wherein a given power plate and a given ground plate is spaced apart in a range from about 0.1 mils to about 0.5 mils.

20. The power socket according to claim 17, wherein the capacitor includes an inter-digital configuration including a plurality of power and ground plates, and the capacitor further including:

a series of alternating power and ground connectors disposed orthogonal to the power and ground plates.

21. The power socket according to claim 17, wherein the capacitor includes an inter-digital configuration including a plurality of power and ground plates, and the capacitor further including:

a series of four alternating power and ground connectors disposed orthogonal to the power and ground plates on a first side of the capacitor; and

a series of four alternating power and ground connectors disposed orthogonal to the power and ground plates on a second side of the capacitor, wherein the second side is opposite the first side.

22. The power socket according to claim 17, wherein the capacitor includes an inter-digital configuration including a plurality of power and ground plates, and the capacitor further including:

a series of four alternating power and ground connectors disposed orthogonal to the power and ground plates on a first side of the capacitor; and

a series of four alternating ground and power connectors disposed orthogonal to the power and ground plates on a second side of the capacitor, wherein the second side is

opposite the first side, and wherein a given power connector on the first side is aligned opposite a given ground connector on the second side.

23. The power socket according to claim 17, wherein the socket platform includes a first edge and a second edge that are parallel with the major planar surface, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, and wherein the two ground terminals are symmetrically disposed along the second edge.

24. The power socket according to claim 17, wherein the socket platform includes a first edge and a second edge that are parallel with the major planar surface, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, wherein the two ground terminals are symmetrically disposed along the second edge; and

wherein the capacitor that is vertically oriented to the major planar surface is disposed between one of the power terminals and one of the ground terminals.

25. The power socket according to claim 17, wherein the socket platform includes a first edge and a second edge that are parallel with the major planar surface, wherein the power terminal includes two power terminals, wherein the ground terminal includes two ground terminals, wherein the two power terminals are symmetrically disposed along the first edge, wherein the two ground terminals are symmetrically disposed along the second edge; and

wherein the capacitor that is vertically oriented to the major planar surface and is disposed either between the two power terminals or the two ground terminals.

26. A method of operating a device, comprising:

passing a current through a power socket, wherein an alternating first current passes in a first direction through a first capacitor plate that is configured in a plane collinear with the first direction;

wherein a direct second current passes in the first direction through a power terminal;

wherein the alternating first current discharges into a second capacitor plate in a second direction that is substantially opposite to the first direction, wherein the second capacitor plate is spaced apart and immediately adjacent the first capacitor plate; and

wherein the direct second current passes to ground through a ground terminal in the second direction.

27. The method according to claim 26, wherein the first capacitor plate and the second capacitor plate are interdigitally configured.

28. The method according to claim 26, further including:

while increasing frequency in a power signal, initiating a lowered inductance path through the first capacitor plate and the second capacitor plate.

ABSTRACT OF THE INVENTION

The present invention relates to a power socket for a microelectronic device that, in one embodiment, uses a low-resistance power and ground terminal configuration. In another embodiment, a low-resistance power and ground terminal configuration is combined on the power socket with a vertically oriented interdigital capacitor that is used to lower inductance. By this combination a significantly lowered impedance is achieved during operation of the microelectronic device.

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Date of Deposit: December 21, 2001
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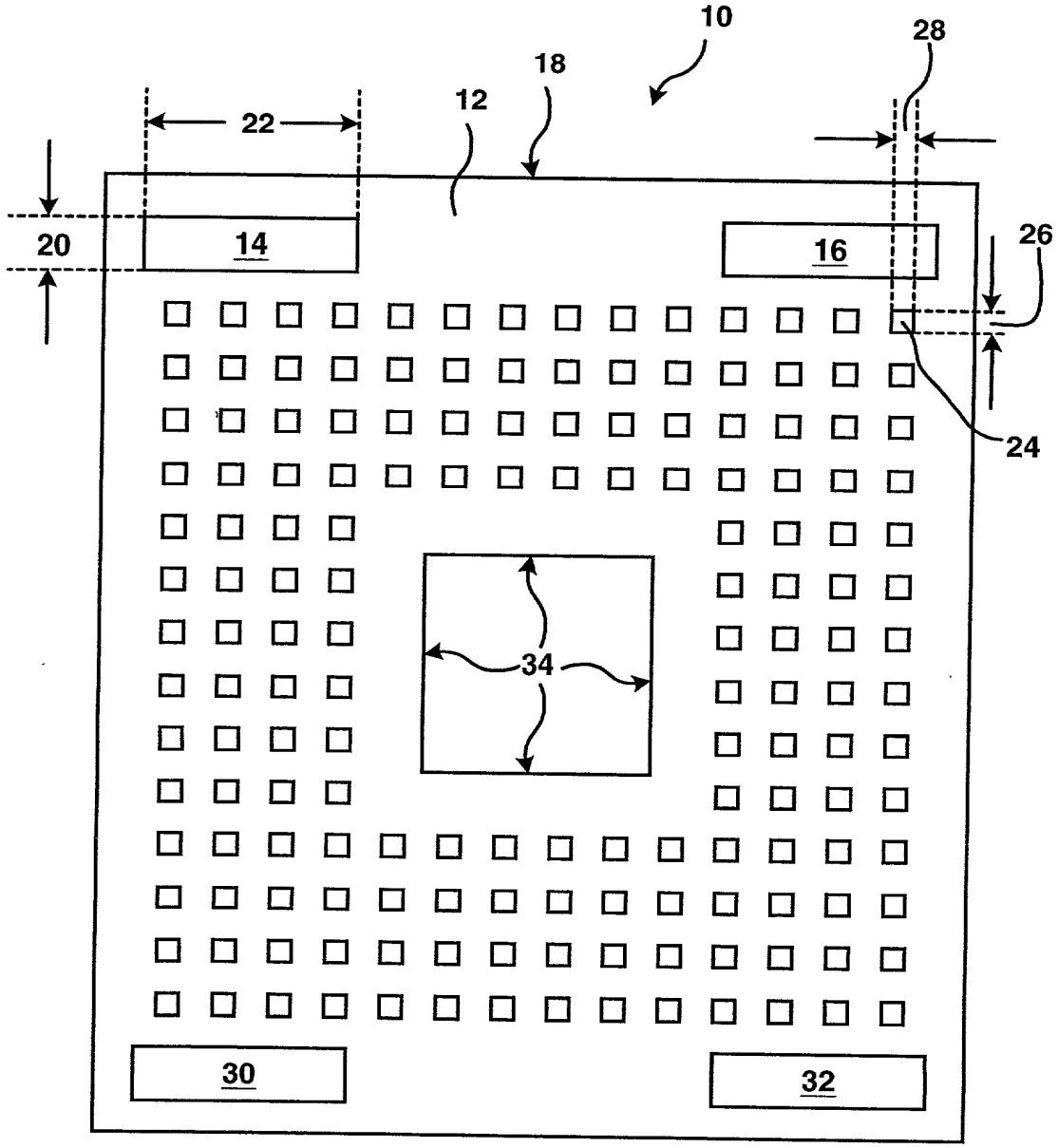

FIG. 1

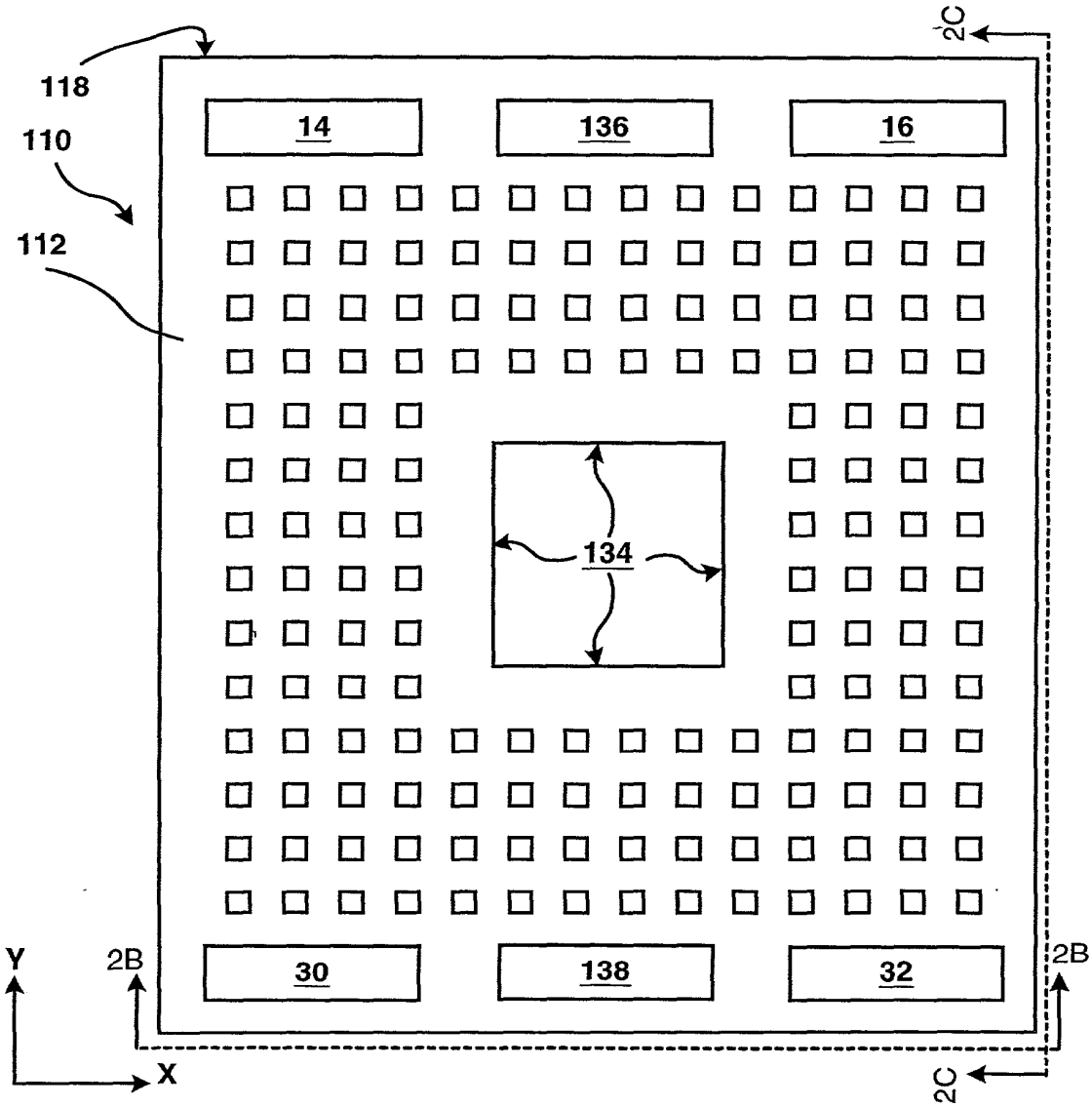

FIG. 2A

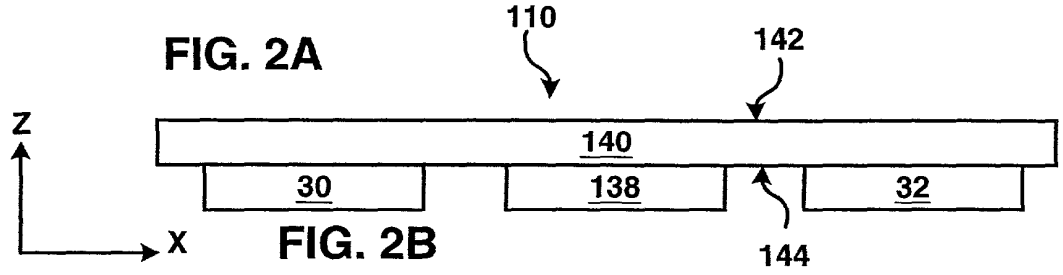

FIG. 2B

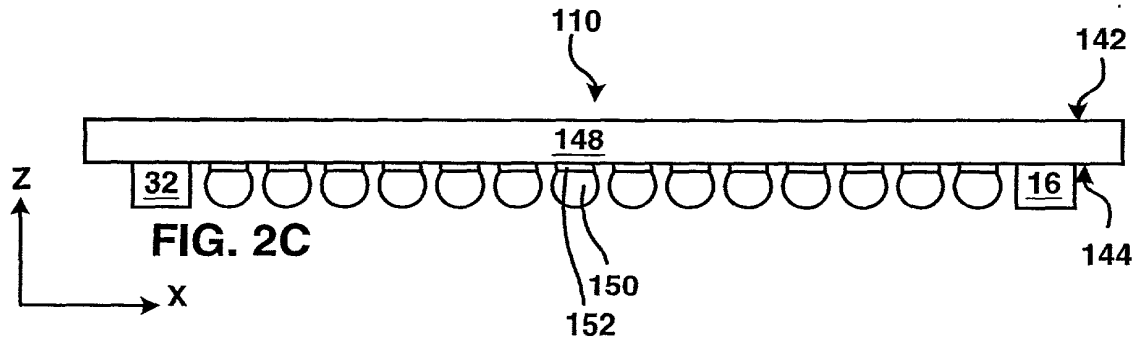

FIG. 2C

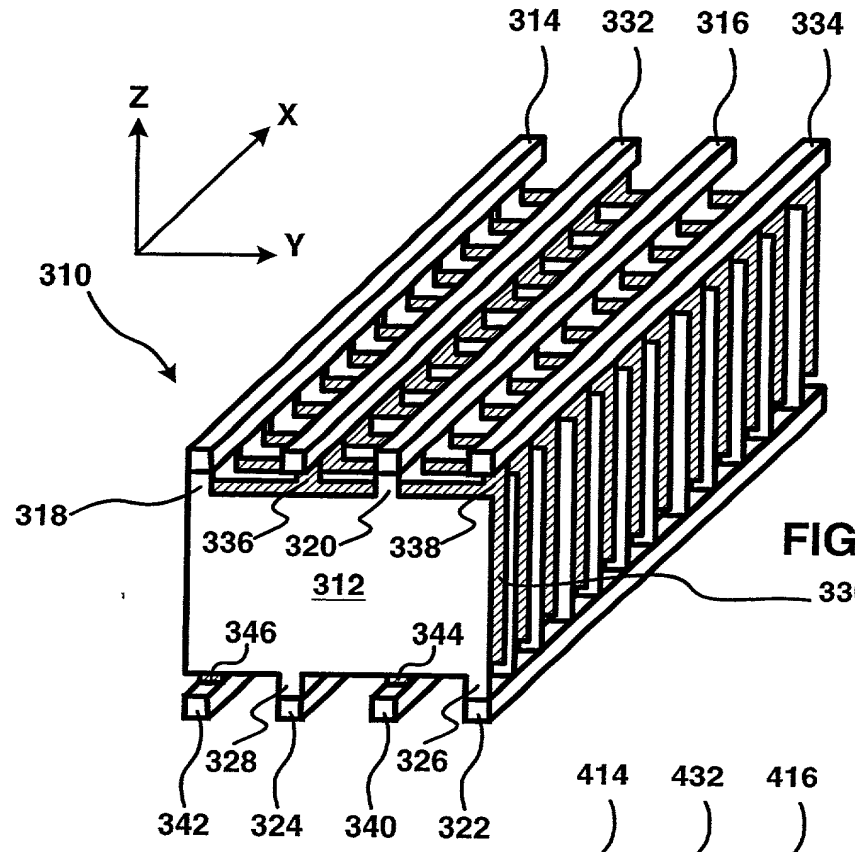
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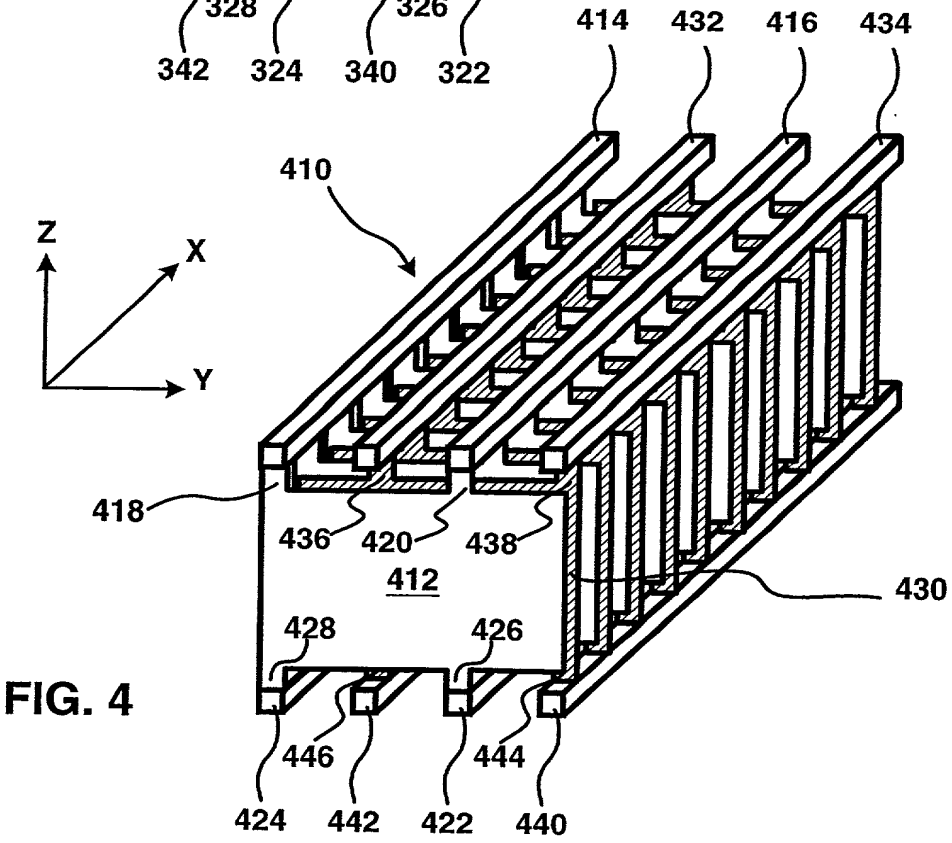
FIG. 3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432
416
434
410
Z
X
Y
418
436
420
438
412
430
428
426
446
444
424
442
422
440

FIG. 4

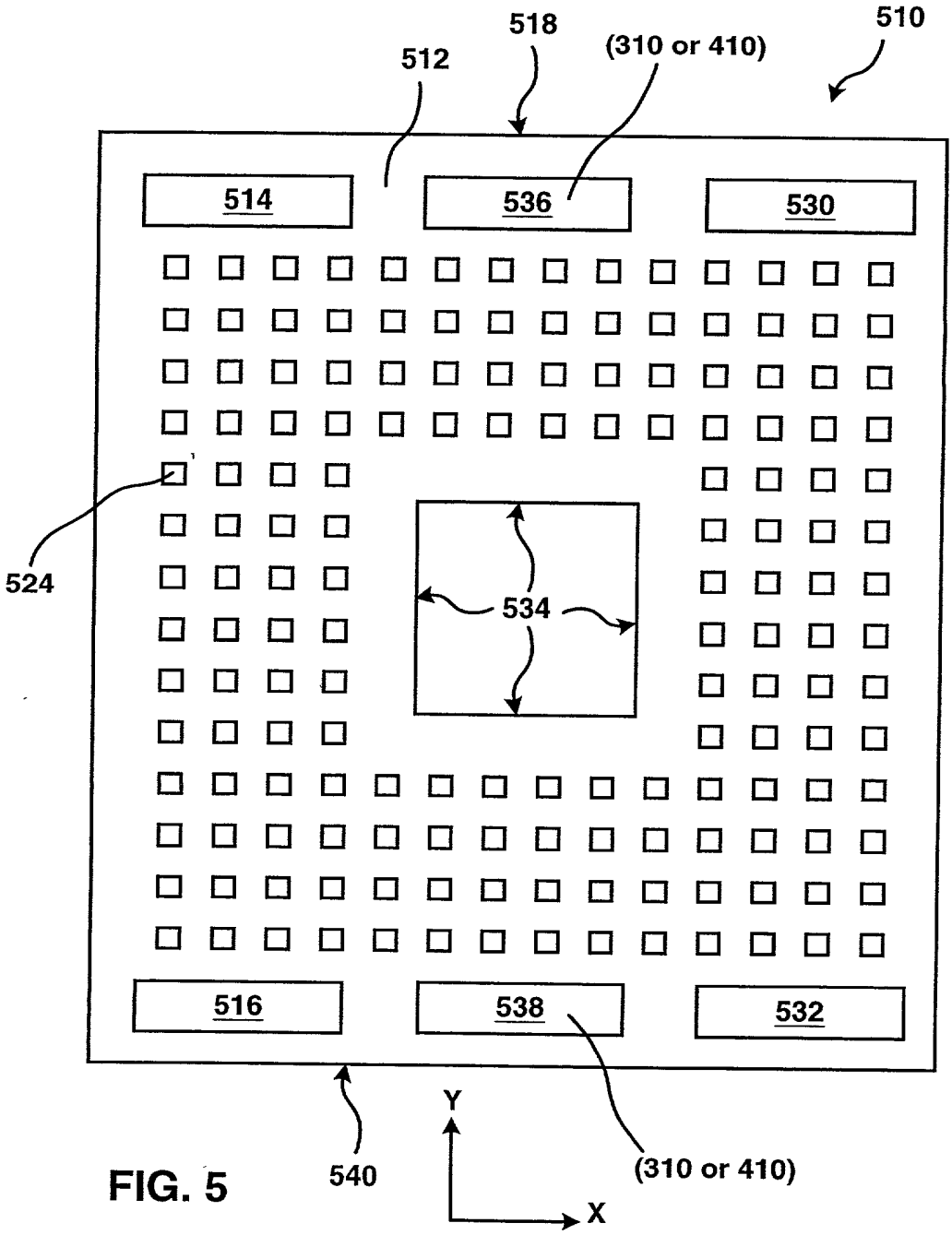
510
518
512
(310 or 410)
514
536
530
524
534
516
538
532
540
(310 or 410)
Y
X

FIG. 5

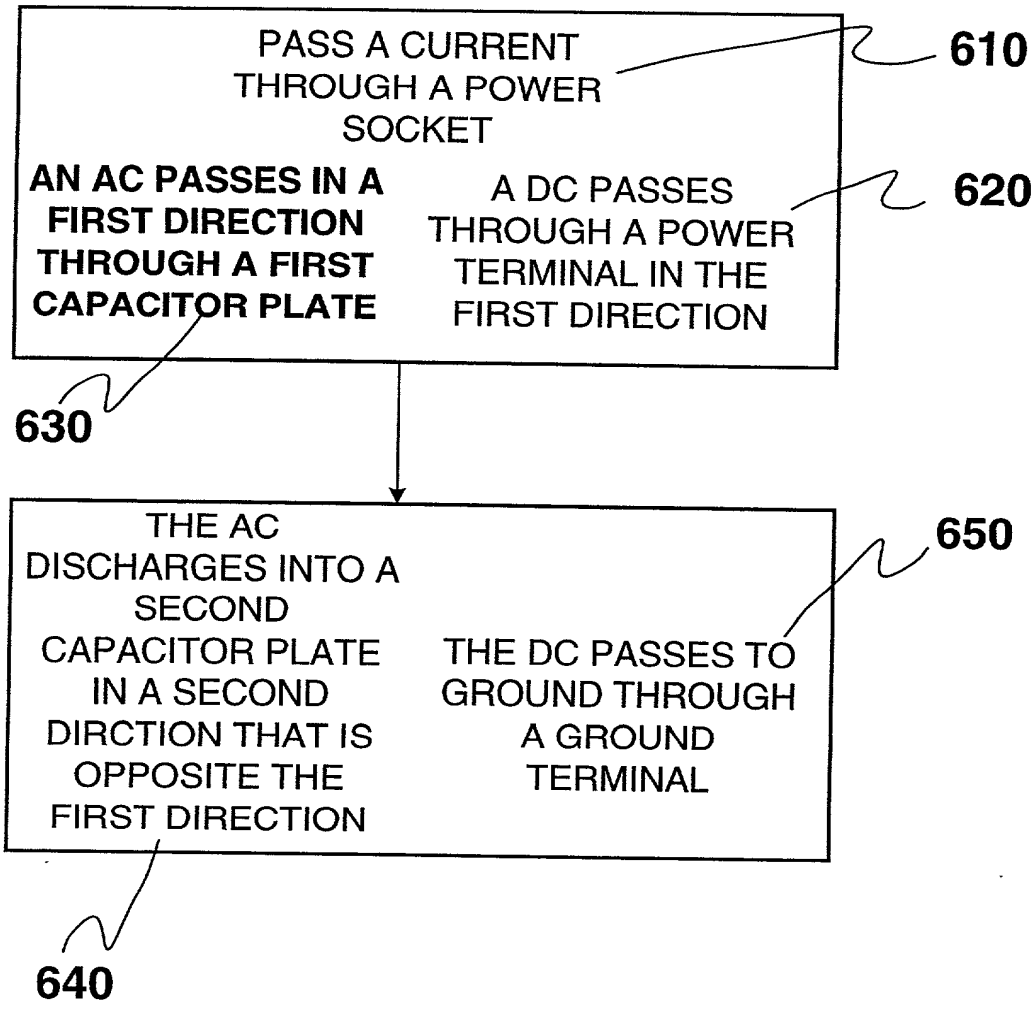
PASS A CURRENT THROUGH A POWER SOCKET
610
AN AC PASSES IN A FIRST DIRECTION THROUGH A FIRST CAPACITOR PLATE
A DC PASSES THROUGH A POWER TERMINAL IN THE FIRST DIRECTION
620
630
THE AC DISCHARGES INTO A SECOND CAPACITOR PLATE IN A SECOND DIRCTION THAT IS OPPOSITE THE FIRST DIRECTION
650
THE DC PASSES TO GROUND THROUGH A GROUND TERMINAL
640

FIG. 6

SCHWEGMAN ■ LUNDBERG ■ WOESSNER ■ KLUTH

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **LOW IMPEDANCE, HIGH-POWER SOCKET AND METHOD OF USING**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

☐ I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. § 1.56 (attached hereto). I also acknowledge my duty to disclose all information known to be material to patentability which became available between a filing date of a prior application and the national or PCT international filing date in the event this is a Continuation-In-Part application in accordance with 37 C.F.R. §1.63(e).

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

☐

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 120 or 365(c) of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

No such claim for priority is being made at this time.

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Aldous, Alan K.	Reg. No. 31,905	Hill, Stanley K.	Reg. No. 37,548	Padys, Danny J.	Reg. No. 35,635
Anglin, J. Michael	Reg. No. 24,916	Huter, Jeffrey B.	Reg. No 41,086	Park, Ellen	Reg No. 34,055
Arora, Suneel	Reg. No. 42,267	Jackson Huebsch, Katharine A.	Reg. No. 47,670	Parker, J. Kevin	Reg. No. 33,024
Beekman, Marvin L.	Reg. No. 38,377	Jurkovich, Patti J.	Reg. No. 44,813	Perdok, Monique M.	Reg. No. 42,989
Berdie, Raymond R.	Reg. No. P-50,769	Kacvinsky, John	Reg. No. 40,040	Peret, Andrew R.	Reg No. 41,246
Bianchi, Timothy E.	Reg. No. 39,610	Kalis, Janal M.	Reg. No. 37,650	Peterson, David C.	Reg. No. 47,857
Billion, Richard E.	Reg. No. 32,836	Kalson, Seth Z.	Reg. No. 40,670	Prout, William F.	Reg. No. 33,995
Black, David W.	Reg. No. 42,331	Kaplan, David J.	Reg. No. 41,105	Reynolds, Thomas C.	Reg. No. 32,488
Brake, R. Edward	Reg. No. 37,784	Klima-Silberg, Catherine I.	Reg No. 40,052	Schumm, Sherry W.	Reg. No. 39,422
Brennan, Leoniede M.	Reg. No. 35,832	Kluth, Daniel J.	Reg. No. 32,146	Schwegman, Micheal L.	Reg. No. 25,816
Brennan, Thomas F.	Reg. No. 35,075	Lacy, Rodney L.	Reg. No. 41,136	Scott, John C.	Reg. No. 38,613
Brooks, Edward J., III	Reg. No. 40,925	Lam, Peter	Reg. No. 44,855	Seddon, Kenneth M.	Reg. No. 43,105
Burge, Ben	Reg. No. 42,372	Lemaire, Charles A.	Reg. No 36,198	Seeley, Mark	Reg. No. 32,299
Burtzlaff, Robert A.	Reg. No. 35,466	LeMoine, Dana B.	Reg. No. 40,062	Skabrat, Steven P	Reg No. 36,279
Calderwood, Richard C.	Reg. No. 35,468	Lundberg, Steven W.	Reg No. 30,568	Skaist, Howard A.	Reg. No. 36,008
Chadwick, Robin A.	Reg. No. 36,477	Maki, Peter C.	Reg. No. 42,832	Smith, Michael G.	Reg. No. 45,368
Clark, Barbara J.	Reg. No. 38,107	Malen, Peter L.	Reg. No. 44,894	Speier, Gary J.	Reg. No. 45,458
Clise, Timothy B.	Reg. No. 40,957	Mates, Robert E.	Reg. No. 35,271	Steffey, Charles E.	Reg. No. 25,179
Cochran, David R.	Reg. No. 46,632	McCrackin, Ann M.	Reg. No. 42,858	Stewart, Steven C.	Reg. No. 33,555
Dahl, John M.	Reg. No. 44,639	McTavish, Hugh E.	Reg. No. 48,341	Stordal, Leif T.	Reg. No. 46,251
Draeger, Jeffrey S.	Reg. No. 41,000	Mehrle, Joseph P.	Reg. No. 45,535	Su, Gene I.	Reg. No. 45,140
Drake, Eduardo E.	Reg. No. 40,594	Mirho, Charles A.	Reg. No. 41,199	Terry, Kathleen R.	Reg. No 31,884
Embretson, Janet E.	Reg. No. 39,665	Moore, Charles L., Jr.	Reg. No. 33,742	Tong, Viet V.	Reg. No. 45,416
Faatz, Cynthia Thomas	Reg. No. 39,973	Muller, Mark V.	Reg. No. 37,509	Viksnins, Ann S.	Reg. No. 37,748
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Gamon, Owen J.	Reg. No. 36,143	Nama, Kash	Reg. No. 44,255	Winkle, Robert G.	Reg. No. 37,474
Gorrie, Gregory J.	Reg. No. 36,530	Nelson, Albin J.	Reg. No. 28,650	Woessner, Warren D.	Reg. No 30,440
Gortych, Joseph E.	Reg. No. 41,791	Nicholson, Lea A.	Reg. No. 48,346	Wong, Sharon	Reg No. 37,760
Greaves, John N.	Reg. No. 40,362	Nielsen, Walter W.	Reg. No. 25,539	Yates, Steven D	Reg. No. 42,242
Haack, John L.	Reg. No. 36,154	Novakoski, Leo V.	Reg. No. 37,198	Young, Charles K.	Reg. No 39,435
Harris, Robert J.	Reg. No. 37,346				

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/ firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to **Schwegman, Lundberg, Woessner & Kluth, P.A.** at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402
Telephone No. (612)373-6900

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Citizenship: **China** Residence: **Chandler, AZ**
Post Office Address: 500 N. Metro Blvd.
#2157
Chandler, AZ 85226

Signature: _____ Date: _____
Dong Zhong

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature: _____ Date: _____
Yuan-Liang Li

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Post Office Address: 5025 E. Hilton Avenue
Mesa, AZ 85206

Signature: _____ Date: _____
David G. Figueroa

Full Name of joint inventor number 4 : **Jiangqi He**
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Apt. 103
Chandler, AZ 85226

Signature: _____ Date: _____
Jiangqi He

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.